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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,439	01/30/2004	Nobuhisa Kumamoto	AI 318D1	7225
7590 MR STEVEN M RABIN C/O RABIN & BERDO PC SUITE 500 1101 14TH STREET NW WASHINGTON, DC 20005			EXAMINER CAO, PHAT X	
			ART UNIT 2814	PAPER NUMBER
			MAIL DATE 06/11/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/767,439	KUMAMOTO ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 March 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 11-26 is/are allowed.
- 6) ☒ Claim(s) 27 and 28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 09/504,874.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claim 28 is rejected under 35 U.S.C. 102(e) as being anticipated by Washida et al (US. 5,949,135).

Washida (Fig. 8) discloses a production process for a semiconductor chip, comprising the steps of: providing a first internal interconnection 2f and a second internal interconnection 2d on a semiconductor substrate 1a; forming a surface protective film 10 over the internal interconnections; forming a first opening and a second opening in the surface protective film 10 to respectively expose a portion of the first internal interconnection 2f and a portion of the second internal interconnection 2d; forming a bump (12,13,3j) projecting from the surface protective film 10 on the portion of

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the first internal interconnection 2f exposed through the first opening; and forming, simultaneously with the formation of a part 12 of the bump (12,13,3j), a surface interconnection (corresponding to the end portion of layer 12) electrically connected to the bump and also electrically connected to the second internal interconnection 2d through the second opening, the surface interconnection having a smaller height than the bump (12,13,3j) and having a thickness that is substantially uniform.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Washida et al (US. 5,949,135) in view of Mori (US. 5,604,379).

Washida (Fig. 8) discloses a production process for a semiconductor chip, comprising the steps of: providing a first internal interconnection 2f and a second internal interconnection 2d on a semiconductor substrate 1a; forming a surface protective film 10 over the internal interconnections; forming a first opening and a second opening in the surface protective film 10 to respectively expose a portion of the first internal interconnection 2f and a portion of the second internal interconnection 2d; forming a bump (12,13,3j) projecting from the surface protective film 10 on the portion of the first internal interconnection 2f exposed through the first opening; and forming, simultaneously with the formation of a part 12 of the bump (12,13,3j), a surface

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interconnection 12 electrically connected to the bump and also electrically connected to the second internal interconnection 2d through the second opening, the surface interconnection 12 having a smaller height than the bump (12,13,3j).

Washida does not disclose that the surface interconnection 12 is formed by electroplating.

However, Mori (Fig. 3) teaches a process of forming a conductive bump structure for a semiconductor chip, the conductive bump structure comprising a surface interconnection 5 which is formed by using electroplating process (column 5, lines 18-21). Accordingly, it would have been obvious to form the surface interconnection 12 of Washida by using electroplating process because such process is well known for forming the metal wiring for the semiconductor device, as taught by Mori (column 5, lines 18-21).

Allowable Subject Matter

5. Claim 11-12 and 25-26 are allowed. The withdrawn claims 13-24 are also allowed because they directly or indirectly depend from allowable independent 1. Therefore, claims 11-26 are allowed.

Response to Arguments

6. With respect to new claim 27, In response to Applicant's argument that Washida does not suggest the step of forming the surface interconnection comprising electroplating, the new reference is applied in the new ground of rejection.

With respect to new claim 28, Applicant argues that Washida does not suggest the surface interconnection having a substantially uniform thickness.

This argument is not persuasive because if the end portion of the layer 12 shown in Fig. 8 of Washida is interpreted as "a surface interconnection" then the end portion of the layer 12 or "a surface interconnection" has a substantially uniform thickness.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

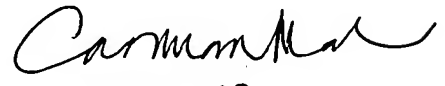
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PC
June 6, 2007


PHAT X. CAO
PRIMARY EXAMINER